REMARKS

In view of the following remarks, reconsideration is requested.

Claims 1, 7, and 9 have been amended to ensure that the claims are construed to read that the at least one floating gate is between the control gate or gates and the active channel, and not between a plurality of control gates. Claim 2 has been amended, and new claim 16 added to ensure that the claims are construed to read that the diodes are reverse biased and that diodes implemented with transistors are reverse biased. A minor editorial amended has been made to claim 10. Claims 17-19 have been added to recite the subject matter of claims 13-15, respectively, but to depend on claim 16, which includes a recitation previously found in claim 2.

Claims 7-12 were allowed. It is submitted that the amendments to claims 7, 9, and 10 do not affect the allowability of claims 7-12. Claims 2, 4, 6, and 13-15 were indicated to be allowable if rewritten in independent form. It is submitted that the amendments to claim 2 do not affect the allowability of claims 2, 4, 6, and 13-15. Moreover, it is submitted that new claims 16-19 are allowable for the same reasons as claims 2, and 13-15.

Claims 1, 3, and 5 were rejected under 35 USC 102(b) as being anticipated by Sridhar. This rejection is traversed for the following reasons.

Claim 1 recites a floating gate MOSFET in which a floating gate is coupled by first and second non-linear resistances to first and second control voltage sources respectively. Claim 1 further recites that the resistances form a voltage divider network that sets the operating voltage of the floating gate.

Sridhar discloses an apparatus for programming an analogue synapse, and neural networks incorporating such synapses. As illustrated in Figure 1 of Sridhar, the analogue synapse comprises two floating gate MOSFETs 10, 11. A pair of analogue switches 12, 13 produce charge that is injected by tunnelling means into the floating gate of each MOSFET 10, 11. The analogue switches 12, 13 each comprise a P-type MOSFET and a N-type MOSFET. The examiner equates the invention recited in claim 1 with one of the two branches of the circuit of Sridhar, e.g. the floating gate MOSFET 10, and the switch 12.

The Examiner asserts that the MOSFETs that make up an analogue switch of Sridhar

represent non-linear resistances that couple the floating gate to first and second control voltage sources. This interpretation is not correct. In Sridhar, the MOSFET gate voltages 34, 35 are never coupled to the floating gate. Rather, the gate voltages modulate the channel beneath the respective gates. The floating gate might be said to be coupled via the pair of MOSFETs to a voltage present on the programming line, but in that case there is only a single voltage and not first and second voltages as recited in claim 1.

The examiner's conclusion that the first and second non-linear resistances of Sridhar (i.e. the MOSFET pair 40,42) form a voltage divider network which sets the operating voltage of the floating gate is also incorrect. Even if the voltages on the lines 34 and 35 of Sridhar were coupled to the floating gate, which they are not, both control voltages would not be on at the same time so as to form a voltage divider network. It is clearly fundamental to the design of Sridhar that only one control voltage is on at a time. If both voltages were on at the same time, the net result would be that no current would be sunk from or sourced to the floating gate.

The invention recited in claim 1 overcomes problems associated with using a single reverse bias diode to create a leakage path to the floating gate (i.e. as described in the paper by Shibata), where the reverse biased diode acts as a very large non-linear resistor to create the leakage path required. In such an arrangement, sufficiently large perturbations of the input signal can forward bias the pull-up diode and thereby introduce severe distortion into the device performance. The invention recited in claim 1 solves this problem by using a second non-linear resistance to create a voltage control circuit that will be immune to perturbations in the input signal.

On the contrary, Sridhar solves an unrelated problem and thus does not disclose or suggest the invention recited in claim 1. Indeed, Sridhar suffers from the problem of all conventional floating gate devices, that is charge leakage from the floating gate, and does not provide any disclosure of solving this problem.

In view of the above comments, it is clear that claims 1, 3, and 5 are not anticipated by Sridhar. Accordingly, it is submitted that claims 1-19 are allowable over the prior art of record and that the application is in condition for allowance.

The Examiner is invited to contact the undersigned by telephone to resolve any remaining issues.

Respectfully submitted,

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